NanoSpice

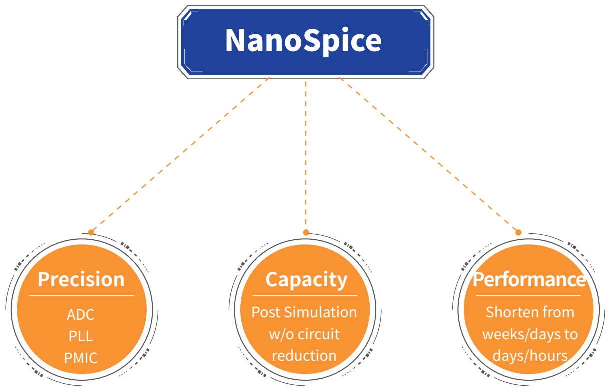
PRIMARIUS

Universal Parallel SPICE Simulator

Introduction

NanoSpice is a new generation of high-capacity, high-performance parallel SPICE simulator. NanoSpice is designed for the most challenging simulation jobs, such as large post-layout analog circuit simulations requiring high capacity, speed and accuracy, all at the same time.

NanoSpice superior parallelization technologies enable efficient circuit simulation with up to 50 million circuit elements. This unique advantage of NanoSpice enables it to deliver better performance than other SPICE simulators for high precision simulation. NanoSpice also features an innovative parallelization license model that offers a cost-effective choice for designers.



Key Advantages

- Accuracy
  Pure SPICE engine, following the highest industry standard
- Capacity
  Larger capacity than other SPICE without circuit reduction
- Performance
  2X+ faster than other solutions with the same precision
- Compatibility
  Standard input/output formats and fully compatible SPICE features
- Foundry validated accuracy
  Proven in mature for 16/14/7/5/3nm FinFET & FD-SOI processes

Application Examples

Circuit	Type	Simulation	Element No. in Circuit	Reference (16T)	NanoSpice (16T)	Speedup
SH+PGA+ADC	Post	Trannoise	MOS:123138 Res: 5 Cap: 554916	72h	13.5h	5.3X
PGA	Post	Trannoise	MOS:411 Res: 17 Cap: 897	0.9h	0.78h	1.1X
PGA+ADC	Post	Trannoise	MOS:5822 Res: 15 Cap: 914	9h	3.5h	2.5X

Circuit	Type	Simulation	Element No. in Circuit	Reference (6T)	NanoSpice (6T)	Speedup
RAMP	Post	Transient	MOS:76691 Res: 2091752 Cap: 778121	110h	43h	2.5X
CDS	Pre	Transient	MOS:38526 Res: 929 Cap: 18804	5.6h	0.72h	7.8X
CDS	Post	Transient	MOS:675606 Res: 25792 Cap:1482936	12.4h	3.7h	3.3X
PLL	Post	Transient	MOS:2787 Res: 28597 Cap: 17075	7.3h	1.4h	5.4X

Specifications

- Supports HSPICE and Spectre netlist formats
- Supports all public domain models, user-defined models
  - MOSFET: BSIM3, BSIM4, BSIM-BULK, BSIM-IMG, BSIM-CMG, BSIM-SOI, LETI-UTSOI, PSP, HiSIM2, HiSIM_HV, EKV3
  - BJT: MAXTRAM, VBIC, HICUM; TFT: a-Si TFT, poly-Si TFT
  - Diode: JUNCAP, JUNCAP200, DIODE_CMC; Varactor: MOSVAR
  - Resistor: R2_CMC, R3_CMC; HEMT: ASM-HEMT; JFET/MESFET; TMI/Custom PMI; Bsource
- Full SPICE analysis features
  - OP, DC, AC, Noise, Transient, Trannoise, FFT, Sweep, Alter, Bisection Stability, Pole-Zero, Monte Carlo, DC Match, AC Match
- Supports Verilog-A (LRM2.4) and behavioral sources
- Supports VEC and VCD stimulus files
- Supports standard output formats for data analysis: FSDB, PSFASCII, SPICEASCII, ASCII, etc
- Supports S-parameter, Transmission line (W element, T element), IBIS model
- Supports SPEF, DSPF, DPF back-annotation
- Supports statistical analysis such as PVT, Monte Carlo, high-sigma
- Drop-in replacement of any SPICE simulator in existing design flows for any transistor-level circuit simulations
- Support public cloud platform, hybrid cloud and private cloud

Applications

- Analog circuit, full customized digital circuit and mixed-signal circuit simulation and verification
- Standard Cell characterization and verification
- Memory circuits characterization and verification