PadInspector

PRIMARIUS

Chip-to-Package Connectivity Verification Solution

Introduction

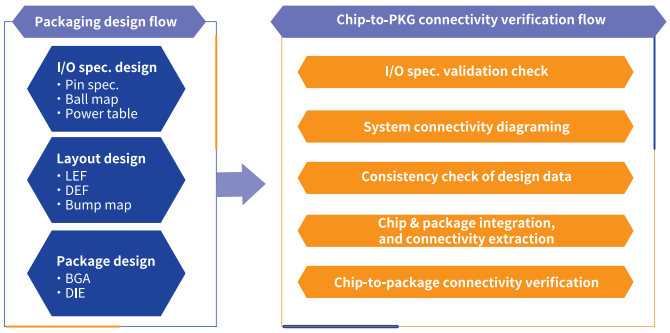
As the complexity of SoC design is increasing rapidly to meet high-performance requirements, the number of components is growing exponentially in SoC design. Since I/O pad configuration planning and chip-to-package connectivity verification with package design are required earlier than traditional design methodology, it is becoming a crucial issue for time-to-market in the SoC industry.

In addition, the automated and standardized task of verifying system connectivity from I/O pads to ball on the package has not been done, so it causes many errors & defects. Accordingly, it is necessary to establish seamless and robust chip-topackage connectivity verification methodology, as well.

PadInspector is an unique and robust chip-to-package connectivity verification solution. It enables to verify integrated system connection with extraction of the connectivity between chip and package design.

Recently, system packaging has been manufactured in various types. Accordingly, PadInspector supports the following packaging options to meet this diversity.

- Flip-chip
- Wire-bonding
- PoP (Package on package)
- SiP (System in Package) & MCP (Multiple chip package)
- 2.5D



Specifications

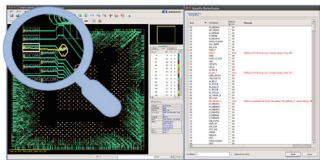
- I/O specification validation check
- Chip-to-package connectivity verification
- Consistency check of heterogenous design data
- Diagraming of system connectivity between chip & package
- Extraction & integration of the connectivity between chip & Package

Applications

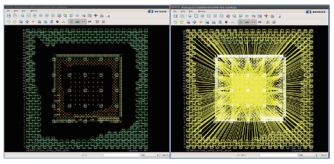
- Package designing interface
- Back-end designing with RDL
- IO pad & bump configuration planning

Application Examples

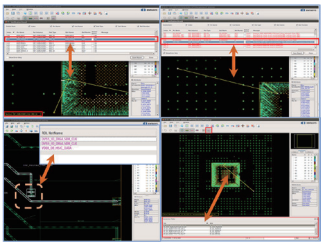
Pad to bump connectivity extraction & design consistency check



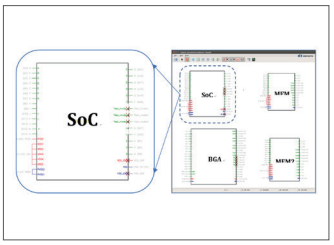
Chip & package design integration



Chip & package design integration



Chip & package connectivity diagram



Key Advantages

- Achieve error-free chip-to-package connectivity engagement for PKG design
- GUI based easy and convenient error debugging environment
- User-oriented chip-to-package specification
- Fast debugging TAT and reduce long design iteration
- Support various package type
- Efficient communication method